GUI req V1.1

1：top

A: Operation voltage： 可写框，从8V~24V；一位小数

写 reg0c [3:2]

|  |  |
| --- | --- |
| Operation\_Voltage[1:0] | operation voltage 01:15~24V 10:10~14.9V 11:8V~9.9V |

B: mode config

下拉菜单：2.0/2.1/PBTL 中选一个 [Jun]: **1. reg20 bit[7] 找不到 2. 2.0 和PBTL一样？？**

选这些值操作寄存器;

2.0: reg05 [2]=0; reg20 byte1[7] = 1; reg20 byte1[3] = 1; reg1A [7] = 1; reg11=0xb8;reg12=0x60;reg13=0xa0;reg14=0x48;

2.1: reg05 [2]=1; reg05 [3]=1; reg1A [7] = 1; reg11=0xb8;reg12=0x60;reg13=0xa0;reg14=0x48;

PBTL: reg05 [2]=0; reg20 byte1[7] = 1; reg20 byte1[3] = 1; reg1A [7] = 1; reg11=0xb8;reg12=0x60;reg13=0xa0;reg14=0x48;

C: interface config

1）下拉菜单：I2S/LJ/RJ 中选一个

2）下拉菜单：16/20/24 bit 中选一个

写寄存器0x04[3:0]

|  |  |  |
| --- | --- | --- |
| [3:0] | AIF\_FORMAT[3:0] | audio interface data format 4'b0000: Right-Justified 16bit 4'b0001: Right-Justified 20bit 4'b0010: Right-Justified 24bit 4'b0011: I2S-Justified 16bit 4'b0100: I2S-Justified 20bit 4'b0101: I2S-Justified 24bit 4'b0110: Left-Justified 16bit 4'b0111: Left-Justified 20bit 4'b1000: Left-Justified 24bit |

C: Operation Status （按下refresh；读寄存器，更新数据）

1）Sample Rate；数据框； 读寄存器0x00[7:5] / 0x00[1:0]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0x00 | Clock control register | [7:5] | FS\_SEL[2:0] | show the auto detect-ed sample rate (also refer to FS\_128k and Fs\_64k) 3'b000: Fs=32k;  3'b001: Fs=192k;  3'b010: Fs=96k;  3'b011: Fs=44.1k/48k;  3'b100: Fs=16k;  3'b101: Fs=22.05k/24k;  3'b110: Fs=8k;  3'b111: Fs=11.025k/12k; |
| [4:2] | MCLK\_FREQ[2:0] | show the auto detect-ed MCLK(or BCLK if PLL source select BCLK) to WS ratio 3'b000: 64 x Fs  3'b001: 128 x Fs  3'b010: 192 x Fs  3'b011: 256 x Fs  3'b100: 384 x Fs  3'b101: 512 x Fs  3'b110: Reserved  3'b111: Reserved |
| [1] | FS\_128K | show the auto detect-ed sample rate (also refer to FS\_SEL) 1:Fs = 128k |
| [0] | FS\_64K | show the auto detect-ed sample rate (also refer to FS\_SEL) 1:Fs = 64k |

2: 原点是错误报警；为1红灯；为0绿灯

Refresh， 读0x02寄存器；更新相应位：

Clear ：按钮；对0x02寄存器写0x00，清零改寄存器

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0x02 | Error status register | [7] | MCLK\_ERR | MCLK error indicator 0: No error 1: MCLK error |
| [6] | PLL\_LOCK\_ERR | PLL lock error indicator 0: No error 1: PLL lock error |
| [5] | BCLK\_ERR | BCLK error indicator 0: No error 1: BCLK error |
| [4] | WS\_ERR | WS error indicator 0: No error 1: WS error |
| [3] | FRAME\_SLIP | Frame slip error indicator 0: No error 1: Frame slip error |
| [2] | CLIP\_INDICATOR | Audio clipping indicator 0: No audio clipping 1: Audio Clipping |
| [1] | OC\_OT\_OV\_UV | OC/OT/OV/UV error indicator 0: No error 1: OC/OT/OV/UV error |
| [0] | OTW | OTW indicator 0: No OT warning 1: OT warning |

D: input mux 框；双击弹窗；显示input mux 具体block

1：chl mux

原点标示选择哪条通路

0x20 byte1[6:4]

|  |  |  |
| --- | --- | --- |
| byte1[6:4] | SDIN\_TO\_CH1 | channel 1 source selection channel 1 source select 3'b000: SDIN-L to channel 1 3'b001: SDIN-R to channel 1 others: Ground(0) to channel 1 |

chr mux

原点标示选择哪条通路

0x20 byte1[2:0]

|  |  |  |
| --- | --- | --- |
| byte1[2:0] | SDIN\_TO\_CH2 | channel 2 source selection channel 2 source select 3'b000: SDIN-L to channel 2 3'b001: SDIN-R to channel 2 others: Ground(0) to channel2 |

Subch mux

原点标示选择哪条通路; 0x21 [Jun]: **只有1个bit怎么控制3个状态？**

|  |  |  |
| --- | --- | --- |
| byte2[0] | CH4\_SOURCE\_SEL | channel 4 source selection channel 4 source select 1'b0: (L+R)/2 1'b1: left-channel post BQ |

两个方框中可以写值；初始值0.5 [Jun]: **Todo next**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0x61 | Channel 4 (subchannel) input mixer | byte0[1:0], byte1[7:0], byte2[7:0], byte3[7:0] | CH4\_INPUT\_MIXER\_1[25:0] | channel 4 (sub-channel) input mixer 1 |
| byte4[1:0], byte5[7:0], byte6[7:0], byte7[7:0] | CH4\_INPUT\_MIXER\_0[25:0] | channel 4 (sub-channel) input mixer 0 |

E: Audio process engine框；不可操作；使用Tab来与主界面切换

F: master vol框；音量条；操作暨配置寄存器；mute是勾选框；

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0x07 | Master volume | [7:0] | MASTER\_VOL | Master volume： 00000000: 24dB 00110000: 0dB … 11111110: -103dB 11111111: soft mute |

G:

output mux 框；双击弹窗；显示output mux 具体block

这个框的显示和前面mode config选择相关：操作reg25

当 mode = 2.0时；弹出2.0 的output mux；default的值 reg25=0x01021345；

当 mode = 2.1时；弹出2.1 的output mux； default的值 reg25=0x01012345；

当 mode = PBTL时；弹出PBTL 的output mux ；default的值 reg25=0x01002245；

Output mux中的四个小方框可以是PWMA、PWMB、PWMC、PWMD中任意一个；可出现多次；

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0x25 | PWM output MUX register | byte1[5:4] | MUX\_TO\_OUT\_A | Multiplex to PWM OUT\_A 2'b00: Multiplex PWM1 to OUT\_A 2'b01: Multiplex PWM2 to OUT\_A 2'b10: Multiplex PWM3 to OUT\_A 2'b11: Multiplex PWM4 to OUT\_A |
| byte1[1:0] | MUX\_TO\_OUT\_B | Multiplex to PWM OUT\_B 2'b00: Multiplex PWM1 to OUT\_B 2'b01: Multiplex PWM2 to OUT\_B 2'b10: Multiplex PWM3 to OUT\_B 2'b11: Multiplex PWM4 to OUT\_B |
| byte2[5:4] | MUX\_TO\_OUT\_C | Multiplex to PWM OUT\_C 2'b00: Multiplex PWM1 to OUT\_C 2'b01: Multiplex PWM2 to OUT\_C 2'b10: Multiplex PWM3 to OUT\_C 2'b11: Multiplex PWM4 to OUT\_C |
| byte2[1:0] | MUX\_TO\_OUT\_D | Multiplex to PWM OUT\_D 2'b00: Multiplex PWM1 to OUT\_D 2'b01: Multiplex PWM2 to OUT\_D 2'b10: Multiplex PWM3 to OUT\_D 2'b11: Multiplex PWM4 to OUT\_D |

H: Enable框；使能开关：

Enable时：reg05[6]=0;

Disable时：reg05[6]=1;

I: SYNC框；同步寄存器：

点击回读寄存器；更新界面

J: Back to default框；软件复位：

点击寄存器回到初始状态；